Improvement of Predictive Pulsed Compensation using Adapted Synchronization

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***Abstract*—Within the scope of miniaturization of power electronics in electrical vehicles, the size and weight of required electromagnetic interference (EMI) filter is getting more and more important. Active EMI filters can provide a solution to reduce those two critical parameters. One active EMI filter approach can be Predictive Pulsed Compensation (PPC). Using power electronic components, a compensation pulse is injected to the noisy power lines. The timing and amplitude of this pulse compared to the EMI source of the power converter determines the achievable attenuation of the compensation circuit. Different operating points of the power converter lead to various time delays between the switching signal and the resulting switching event. These delays cause a synchronization error of the compensation pulse related to the power converters' operating point. This paper presents a method to generate an appropriate synchronization signal for adjustment of PPC due to different operation points of the power converter.**

Keywords—Predictive Pulsed Compensation; Active EMI Filter; EMI Filter; EMI Suppression; Electromagnetic Compatibility; EMC; EMI; DC/DC Converter

I. INTRODUCTION

One of the main sources of electromagnetic disturbances in hybrid and electrical vehicles are pulsed power electronic components like DC/DC converters and DC/AC inverters. To fulfill the standards of electromagnetic compatibility (EMC), one method is filtering of disturbed power lines with passive EMI filters. In case of high voltage DC-links in electrical vehicles the permitted Y – capacitance of the common mode filter is limited, due to safety regulations. The required filter attenuation is achieved by larger common mode chokes (CMC) which lead to more bulky and heavy filter components.

Different publications presented active EMI filters as an alternative to conventional passive EMI filters [1]-[4]. By injecting a compensation current (or voltage) disturbances are suppressed. The compensation signal is generated by a sensing circuit and an inverting amplifier [1]. With a combination of active and passive EMI filters, a reduction of size and weight of the EMI filter can be achieved. Due to the limited bandwidth of the active filter, a smaller passive filter is needed to provide the necessary high frequency attenuation. An important disadvantage of active EMI filters are their analog components, which are used to build up the inverting amplifier circuit. Connected to the input terminals of a power converter, the active EMI filter has to withstand conducted immunity tests, for example as described in the ISO 7637 standard or typical surge tests. These immunity tests can only be fulfilled with complex protection circuits, which ads costs and volume [5].

Predictive Pulsed Compensation can be an alternative approach for active EMI filters [6]. Like in conventional active EMI filters, the compensation current is injected to the disturbed power lines. The main difference is the generation of the compensation signal. A rectangular pulse, synchronized to the power converters' switching events, generated by a simple and tiny low power half-bridge module is used as compensation signal, which requires no analog circuits. The performance of the PPC is mainly determined by the timing of the synchronization and the amplitude of compensation pulse [6].

During operation of a power converter, various mechanisms, like different output currents or changes in temperature, are leading to different time delays between the switching command and the actual commutation of the power converter's MOSFETs or Diodes. These different switching delay times have to be considered by the synchronization of the PPCs compensation pulse.

This paper presents a method to generate a suitable signal which can be used to synchronization of the compensation pulse to the actual commutation of the power semiconductors. In the following section II the principle of PPC is explained and the test system is introduced. The extension of the test system for the synchronization is presented in section III. The measurements of the improved PPC system with various operating points are given in section IV. A conclusion is given in section V.

II. PRINCIPLE OF PREDIVTIVE PULSED COMPENSATION

The EMI suppression method called Predictive Pulsed Compensation is introduced in [6]. The idea is to use the information of power converters' control to synchronize a suitable compensation pulse to the EMI source pulse. This compensation method can reduce the power converters emissions below a few MHz significantly [6].

A. *EMI suppression using compensation pulses*

Disturbance signals of pulsed power electronics contain two parts, the harmonics of the switching frequency f_c and resonance effects of parasitic elements. Especially in the lower frequency range, the disturbance spectrum consists of a large number of harmonics and the resulting periodic square wave of the switching event. To reduce the disturbance in this frequency range, only a scaled trapezoidal compensation pulse with the equal harmonic content than the source pulse can be used [6].

Figure 1 depicts the principle of PPC at a simple buck converter application. The switching transition of Q_1 causes a rectangular voltage V_C at the dynamic node C, where the parasitic stray capacitance C_{Par} is summarized. This voltage drop over the stray capacitance causes a common mode ground current flowing through the LISN and back to the buck converter. Using a compensation circuit at the input terminals of the converter, this ground current can be suppressed. Hence, the ratio between V_{Comp} and V_C is determined mostly by the ratio between the capacitors C_{Par}, C_Y and C_{Comp}, a scaled rectangular voltage signal can be used to compensate the ground current [6]. For the frequency range dominated by this capacitive divider ratio, the disturbance signal can be suppressed. In frequency ranges also influenced by inductive effects in the buck converter, the performance of the compensation will degrade.

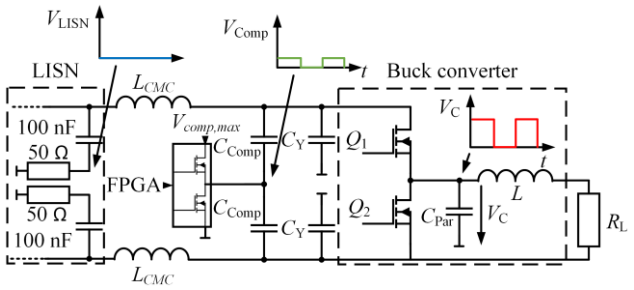

Fig. 1. Equivalent ciruit of the buck converter with integrated PPC circuit

B. *Realization of PPC Hardware*

To realize the PPC hardware, only a few components are required. As coupling capacitors C_{Comp} conventional 10 nF (multilayer ceramic capacitor) MLCC with a Y2-rating are used. The half bridge module for generation of the compensation pulse is realized with a commercial single ended gate driver IC. An adjustable voltage regulator with 12 V input voltage is used for supply. Both, the buck converters' semiconductors and PPC module are controlled by a FPGA platform. This allows a simple synchronization of switching events and compensation pulses.

C. *FPGA Implementation*

Ideal compensation requires both, synchronization of the compensation pulse to the MOSFET switching signal and correction of possible delays of rising and falling edges between switching signal of Q_1 and output voltage pulse V_C. Both edges of the compensation pulse also have to be adjusted separately. To achieve an ideal synchronization, the original PWM signal in the FPGA is used to create the compensation signal. Figure 2 shows the schematic of switching and compensation signal generation implemented on the FPGA. The switching signal for Q_1 is generated by delaying the internal PWM signal. If the time delay of the compensation unit is larger than the switching time delay, it is necessary to start compensation before the switching signal starts.

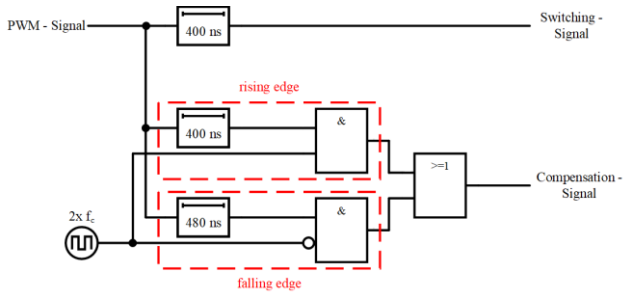

Fig. 2. Generation of the compensation signal on FPGA

The time delays of the rising and falling edges of the compensation pulse are adjusted separately. Therefore, a window signal, with double the carrier frequency of the PWM signal, is used to separate rising and falling edges. Two external adjustable time delays realize the time shift of both edges. By combining both signals, the compensation signal is generated.

III. Sensing of the Exact Switching Event

The main source of EMI is the changing potential over the stray capacitor C_{Par}, like explained in section II a. This change in voltage is linked to the switching signals of MOSFET Q_1 with a varying time delay depending on the current flowing through the MOSFET [7]. For the stationary case, this time delay can be measured and afterwards considered in synchronization of the compensation pulse. For dynamic changes during operation the time delay is also changing and a new measurement of the actual time delay is required for the adaption of the synchronization. During operation, it is difficult to measure the actual time delay and correct the synchronization. An alternative approach can be a sensing circuit at node C, consisting of a capacitive voltage divider in combination with a voltage comparator for creation of a digital synchronization signal. The equivalent circuit extended by the feedback tap is shown in Figure 3. The feedback signal is directly connected with a digital input pin of the FPGA. This feedback tap allows to measure the switching time delay during operation and afterwards adapting the compensation signal dynamically during operation.

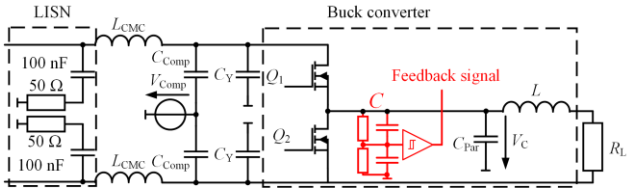

Fig. 3. Extended buck converter with output feedback tap

Obviously, there is also a time delay caused by the comparator circuit which has to be measured and adapted. But this time delay is independent of the power converters' operating point of the power converter and also constant over time. Therefore, it can be compensated statically. The adaption of synchronization is done by changing the time delays of the rising and falling edges, shown in Figure 2. By calculating the difference between the switching signal and feedback signal, the time delay of the switching event is detected with an internal counter and can be expressed as:

$$\Delta t_{\text{switch, rising/falling}} = \Delta(t_{\text{switching signal}}, t_{\text{feedback signal}}) \qquad (1)$$

If the constant delays caused by the comparator and gate driver circuit of the MOSFET Q_1 are subtracted from the detected time difference $\Delta t_{\text{switch, rising/falling}}$, the switching delay

caused by the MOSFET itself can be calculated. This delay is used to correct the time delays of the rising and falling edge in Figure 2.

Furthermore, this feedback signal and the resulting measurement of switching delay could also be used to determine the MOSFET temperature. As described in [8], switching delay of the MOSFET itself is also dependent on the MOSFETs' temperature. By combining the output current with the detected switching delay, a change in junction temperature may be detected. Since this subject is off-topic, temperature measurement using the introduced feedback signal will not be further discussed in this paper.

IV. Practical Demonstration

After the implementation of the adapted synchronization, some measurements were carried out to demonstrate the effect of changing operation points.

A. Test setup

As Device Under Test (DUT) a prototype of a buck converter with Silicon Carbide (SiC) MOSFETs is used. The DUT is enhanced by the PPC hardware, introduced in section II b. With a switching frequency of 49.9 kHz, the buck converter steps the input voltage of V_{In} = 100 V down. The maximum power capability of this setup is 300 W. Due to the measurements, different duty cycles are tested which leads to a varying output voltage of 10 V to 30 V.

The test setup according to CISPR 25 [9] is shown in Figure 4. The equipment is placed on a copper table as ground plane. The DUT is connected to the LISN via two unshielded cables. As power inductor, an external air coil with L = 320 µH inductance is used. An air cooled 33 Ω resistor forms the passive load. The FPGA system and the PPC Unit are supplied by an individual power supply. Hence the PPC Unit suppresses only CM emissions, a power combiner is used to separate the disturbance modes.

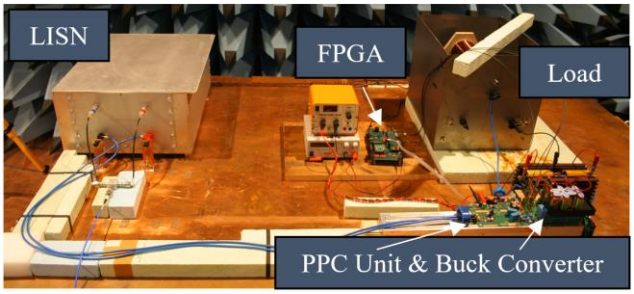

Fig. 4. Test setup of buck converter according to CISPR 25

The measurements of conducted average emissions are taken with an EMI receiver in an extended frequency range from 10 kHz to 30 MHz. To avoid discontinuities in the spectrum, the whole measurement is taken with an internal filter bandwidth of 1 kHz.

B. Switching Behaviour

For a better understanding of the different duty-cycles, switching behaviour is briefly analyzed. The operating points are chosen to be 10% and 30% duty-cycle which results in a mean output current between 0.3 A and 0.9 A. Figure 5 shows the comparison for the Gate – Source voltage V_{GS} (solid lines) of Q_1 and the output voltage V_C (dotted lines) for both duty-cycles. Only the high time of one output voltage pulse is depicted.

For the rising edge, there is a constant deviation in timing between the switching signal of Q_1 and the output voltage V_C of 210 ns. In case of a duty-cycle of 30%, the falling edge has a bigger delay around 280 ns, compared to the rising edge. In case of 10% duty-cycle, on the one hand the delay gets 10 ns larger and on the other hand dV_C/dt is with 0.238 V/ns five times slower compared to 1.22 V/ns at 30% duty-cycle. Due to these effects, the falling edge of the compensation pulse needs to be adjusted, when changing the duty-cycle.

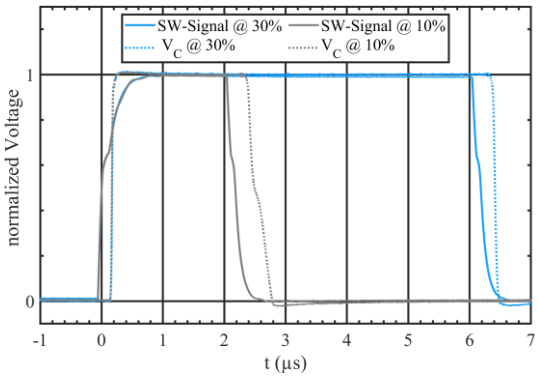

Fig. 5. Q_1's switching signals and output voltage V_C with different duty-cycles

C. Measurement without adapted synchronization

In this section, the measurements of conducted CM emissions of the buck converter with static synchronized PPC are discussed. The PPC unit is manually synchronized at an operation point of 30% duty-cycle and a DC input voltage of 100 V. Figure 6 shows the comparison of the raw CM emissions of the buck converter with deactivated PPC unit (blue) and the buck converter with activated PPC unit (red). With active PPC the fundamental harmonic at 49.9 kHz can be suppressed by 35 dB. The harmonics in the longwave range (LW, 0.15 – 0.3 MHz) can be suppressed by 55 dB – 35 dB. At 1 MHz an attenuation of 31 dB can be achieved. Due to different rise and fall times of source and compensation pulse, an increase of the spectrum of 6 dB – 14 dB is caused above 5 MHz by the compensation pulse.

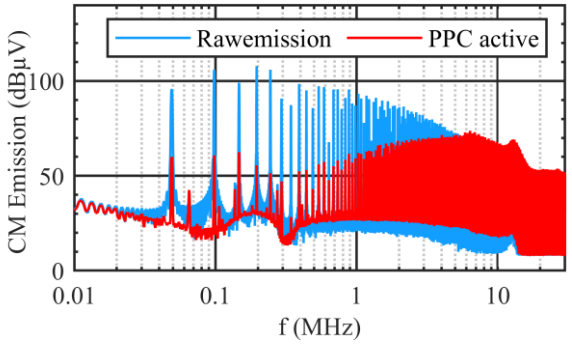

Fig. 6. Measurement of conducted CM emissions without adapted synchronization at 30% duty-cycle

If there is a change in the operating point, the time delays of the compensation also have to be adapted. By using a static synchronized compensation pulse without an adaption of synchronization, a loss in attenuation will occur. This effect is demonstrated with a reduction in duty-cycle down to 10% but with no adaption in synchronization of the compensation pulse. The new spectrum of CM emissions is shown in Figure 7, the raw emissions with deactivated PPC (blue) and suppressed emissions with activated PPC (red). With 31 dB at 49.9 kHz, for the fundamental harmonic there is a loss in attenuation of 4 dB only by changing the duty-cycle without adapting the pulse synchronization. For harmonics in LW the loss in attenuation is between 11 – 32 dB.

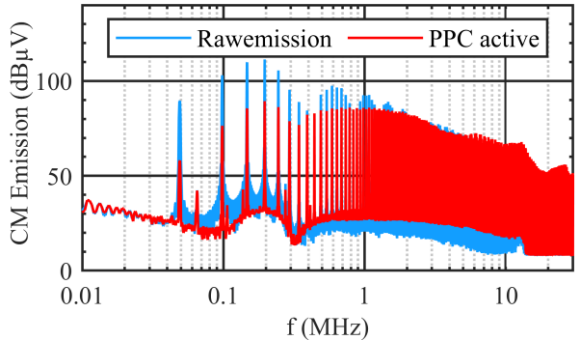

Fig. 7. Measurement of conducted CM emissions without adapted synchronization at 10% duty-cycle

Nevertheless, the rising harmonic content at low frequencies may influence the saturation design of the common mode choke of an additional required passive EMI filter. To avoid the loss in attenuation, an adapted synchronization can be used instead of static synchronization.

D. Measurement with adapted synchronization

In this section, the measurements of conducted CM emissions of the buck converter with automatic synchronized PPC are discussed. The PPC unit is adapted automatically using the feedback signal of the synchronization tap. The comparison of static synchronized PPC of section III c (red) and automatically synchronized PPC (green) are pictured in Figure 8. There is only a slight increase above 100 kHz of 3 – 10 dB. Compared to the high attenuation, which can be achieved with the PPC, this increase can be tolerated. There is only one harmonic at 340 kHz (7^{th} harmonic) with a higher negative impact. Due to the magnitude of the 6^{th} and 8^{th} harmonic, this loss in attenuation is of no consequence.

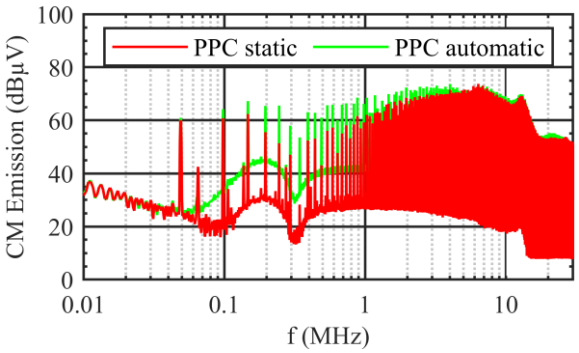

Fig. 8. Measurement of conducted CM emissions with adapted synchronization at 30% duty-cycle

The main advantage of automatic synchronized PPC is the adaption to different operating points. To demonstrate this effect, the measurement with 10% duty-cycle is also done with automatic synchronized PPC, shown in Figure 9. Beside the raw emission (blue) and the static synchronized PPC (red), also the automatically synchronized PPC (green) is measured. By the adaption due to the different duty-cycle, 48 dB attenuation at 49.9 kHz can be achieved. An improvement of 8 dB – 20 dB up to 1 MHz and 3 – 10 dB up to 2 MHz is realized, compared to the static synchronized PPC.

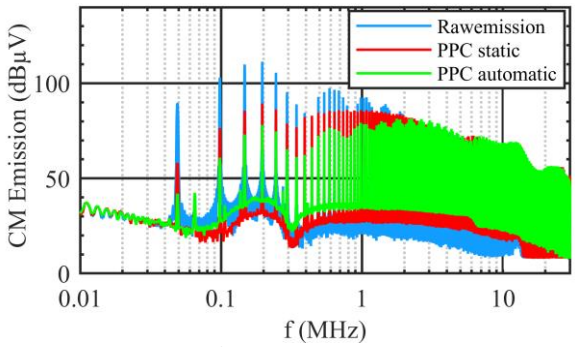

Fig. 9 Measurement of conducted CM emissions with adapted synchronization at 10% duty-cycle

With the automatically synchronized PPC unit a continuously high attenuation can be ensured, even though a changing operating point of the power converter. With respect to an application of PPC for DC/AC inverter, where the sinusoidal output current and thus the switching delays change at each switching event, this method provides a simple solution to adapt the synchronization.

V. Conclusion

This paper presents a new method for an adaption of the necessary synchronization of compensation pulses to the EMI source pulse. Here, a prototype buck converter was used as a demonstrator application. A suitable feedback signal is generated by a capacitive voltage divider in combination with a comparator. This digital signal was used to determine the switching delay of the MOSFET and thus correct the synchronization of the compensation pulse. The implemented extension of the predictive pulsed compensation has been tested at a buck converter application. Measurements have shown a reduction of 35 dB at the fundamental PWM frequency and 55 dB – 35 dB in LW frequency range. Furthermore, the impact of a changing operating point to the performance of the PPC has been demonstrated. By using the developed adaption method, the high attenuation of PPC in frequency range below 1 MHz could be maintained. Beyond that, the adaption can be used for PPC synchronization at a DC/AC converter application, where the timing constraints of compensation pulses are more stringent.

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