Sensitivity Analysis of Behavioral MOSFET Models in Transient EMC Simulation

P. Hillenbrand*, M. Beltle, S. Tenbohlen
Institute of Power Transmission and High Voltage Technology
University of Stuttgart, Germany
*philipp.hillenbrand@ieh.uni-stuttgart.de

S. Mönch
Institute of Robust Power Semiconductor
University of Stuttgart, Germany
stefan.moench@ilh.uni-stuttgart.de

***Abstract*—This contribution investigates behavioral MOSFET models used for the simulation of conducted and radiated electromagnetic interferences (EMI) of an automotive inverter. A combined simulation of an equivalent circuit and the 3D geometry for a traction inverter based on 1.2 kV, 40 A SiC MOSFETs is presented. The model considers the MOSFET as a combination of parasitic elements of the package, voltage-dependent semiconductor capacitances, an internal gate resistance, the IV curves of the MOSFET and the diode. After verifying the model using measurements in the time and frequency domains, it is used to determine the influence of its parameters on the disturbance voltage at the line impedance stabilization network. The results identify the EMI-relevant parameters of the MOSFET and provide information on which data needs to be measured and which can be extracted from the datasheet of the MOSFET.**

Keywords—MOSFET model; traction inverter; EMI; SPICE simulation; transient transistor capacitances

I. Introduction

Recent research has focused on high-density traction inverters in the field of electric vehicles. As more wide-bandgap semiconductor materials become commercially available for switches, the investigation of highly efficient inverters based on SiC and GaN MOSFETs is a rising topic. The advantages of these materials concerning efficiency and thermal stability, and the disadvantages concerning electromagnetic interferences (EMIs) caused by the inverter are intensively discussed in many publications [1,2]. Nowadays, it is recognized that a miniaturization of the converter requires an EMI optimization, because the space needed for the necessary filter requires a considerable proportion of the converter's total volume [2]. Therefore, efficient EMI simulations are an essential part of the inverter's development process.

No matter if the simulation is performed in the time or frequency domain, it needs mostly precise information of all parasitic inductive, capacitive and resistive elements of the test setup, and an accurate model of the semiconductor switches. Focusing only on the MOSFETs used as semiconductor switches, there are plenty of different models available in the literature. They can be grouped into behavioral models [3] and physics-based models [4]. As most of the necessary physical parameters of the switches are not provided by the datasheet and cannot be measured directly at the terminals of the device, behavioral models are often the method of choice. However, it has not yet been shown how the parameter inaccuracies of these models affect the EMI simulation results in the frequency range of 0.15 to 110 MHz in the field of automotive inverters. Which data can be extracted from the datasheet and which require measurements need to be clarified.

In order to fulfill this goal, this contribution uses an existing EMI simulation model for conducted and radiated emissions of a traction inverter in a CISPR25 component test setup. The general simulation approach is shown in Figure 1 and consists of a 3D geometry model of the complete test setup and a circuit simulation of the inverter's commutation cell. Firstly, the necessary parasitic elements of the commutation cell are extracted from the 3D geometry and combined with behavioral models of the switches in a transient simulation program with integrated circuit emphasis (SPICE) simulation. Subsequently, the simulated time domain waveforms of the switches are transformed into the frequency domain and used as excitations in the 3D geometry model. The test setup is similar to the case defined in CISPR25. It

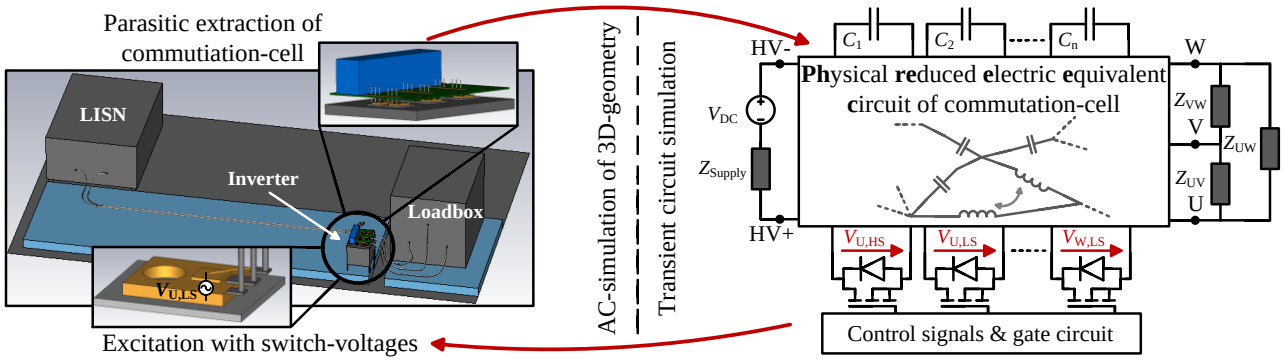

Fig. 1. General simulation approach: Combine the transient circuit simulation of the commutation cell with 3D AC simulation of the complete test setup.

consists of two line impedance stabilization networks (LISNs), the inverter and a three-phase load. All components are mounted on a conductive table and connected to each other with unshielded cables. The MOSFET under investigation is a SCT2080KE SiC MOSFET produced by Rohm with a maximum drain current of 40 A and a breakdown voltage of 1.2 kV. Both the test setup and the 3D geometry AC simulation are well described in [5]. Therefore, this contribution focuses on the transient part of the simulation, which is described in the following section.

II. Transient Circuit Model

A. Behavioral MOSFET model

Figure 2 shows the MOSFET model used, consisting of two voltage-dependent chip capacitances C_{GD} and C_{DS}, one internal gate resistance R_G, a fixed gate-source capacity C_{GS} and two current sources, I_{DS} and I_{SD}, representing the IV curves of the MOSFET and the body diode. Voltage-dependent current sources are directly accessible in SPICE and can be defined as a function of node voltages or currents between nodes. It is essential to use continuous and differenatiable functions for these sources to avoid convergence problems. The voltage-dependent capacitances are not directly accessible in SPICE. Therefore, a capacitor of C_1 = 1 pF is used in combination with one voltage-dependent current source I_C connected in parallel. The current source amplifies the current through C_1. Thereby, C_{DS} appears to be dependent on V_{DS}.

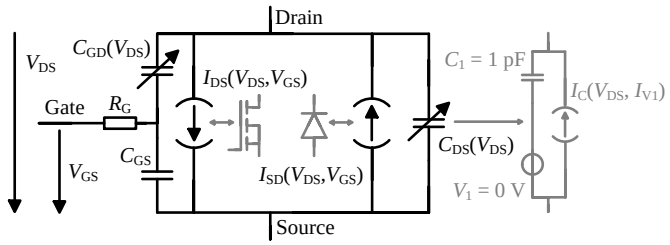

Fig. 2. Circuit elements of the behavioral MOSFET model.

The input data necessary for the model is gained either from the datasheet of the device, from a manufacturer's model or from measurements at room temperature using a B1500A Semiconductor Device Parameter Analyzer (Keysight). The data gained from these sources are compared in Figures 3-5.

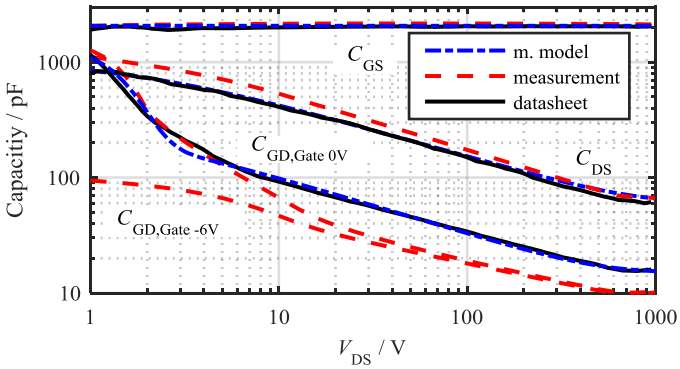

Fig. 3. Comparison of MOSFET capacitances.

Figure 3 shows the static transistor capacitances measured. It shows a substantial difference in the drain-gate capacity C_{GD} measured compared to the datasheet value, and a large dependency of C_{GD} on the gate-source voltage V_{GS}. The influence of this parameter on the EMI of the converter is investigated in section IV. Concerning the IV curves of the MOSFET, Figure 4 shows a very similar shape of the curves in the linear region of the MOSFET at small V_{DS}. The deviations between the measurements and the manufacturer's model become greater in the saturation region of the MOSFET. Unfortunately, most of the datasheets do not offer information about the saturation region at high drain-source voltages, which need a considerable effort to be measured. Thus, measurement uncertainties of this value on the EMI of the converter will be investigated in section V.

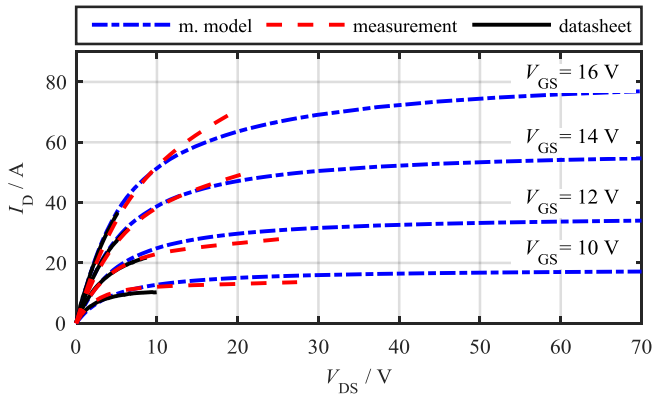

Fig. 4. Comparison of IV curves of the MOSFET in the first quadrant.

The output characteristic of the body diode is pictured in Figure 5. Here, the measurements and the manufacturer's data show similar values for the forward voltage of the diode. However, the measurements show lower diode losses at currents higher than I_S = 2 A and a strong dependency of the forward voltage on the gate-source voltage V_{GS}. The influence of both parameters on the EMI of the converter will be investigated in section VI, where the internal gate-resistance is also varied for the sake of completeness.

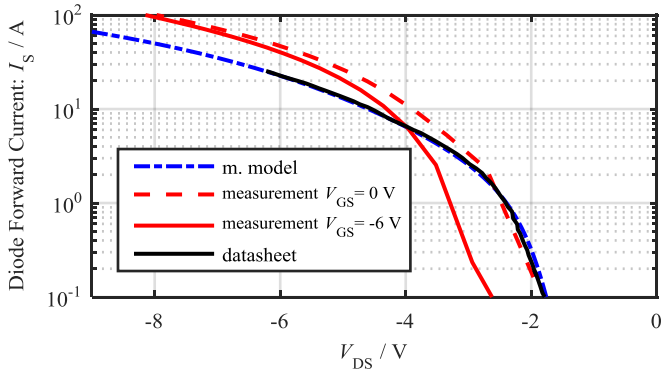

Fig. 5. Comparison of diode output characterisitcs at different gate voltages.

B. Parasitic extraction from 3D geometry

Calculating all the parasitic elements of the gate circuit and the commutation cell is essential for an accurate simulation of the inverter's switching edges. Therefore, a physically reduced electric equivalent circuit is derived from the 3D geometry by

setting nodes at the locations pictured in Figure 6. Partial inductances are obtained between galvanically connected nodes and parasitic capacitances between isolated nodes. As described in [5], the inductances are computed from the eigenmode solution of the geometry model, using the algorithm described in [6]. The capacitances are calculated with an electrostatic solver.

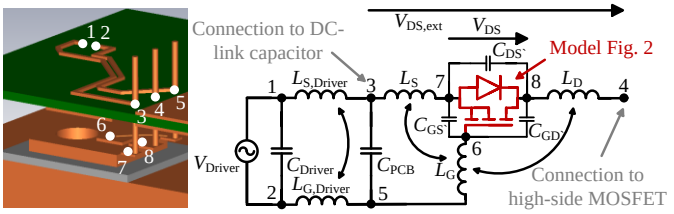

Fig. 6. Computing the necessary parasitic elements from the 3D model.

Figure 6 shows only one low-side MOSFET. The circuit elements and the inductor coupling towards the other MOSFETs and the DC-link capacitors are important and cannot be neglected. However, the inductive and capacitive coupling between adjacent half-bridges is removed to decrease the simulation time.

C. *Equivalent circuit of DC-link capacitor*

This contribution uses the equivalent circuit pictured in Figure 7 to reproduce the frequency-dependent behavior of the DC-link capacitor. The circuit models the imaginary and real part of the DC-link capacitor impedance precisely. Regarding the parametrization, the elements L_{ESL}, C_{Cap} and R_{ESR} are

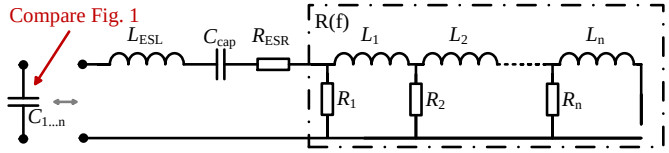

Fig. 7. Equivalent circuit used for DC-link capacitors.

calculated directly from measurements of the DC-link capacitor by using the magnitude of the impedance. L_1 to L_n and R_1 to R_n are fitted values to consider the frequency-dependent losses inside the capacitor.

III. Simulation Results

The transient model described in II is implemented and solved with LT-SPICE V2.3 using the alternate solver. Based

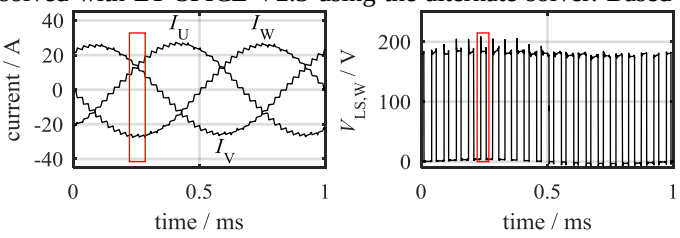

Fig. 8. Time domain simulation result of one load cycle. Left: Load currents of 3~load. Right: V_{DS} of the low-side MOSFET (halfbridge W).

on a sine-triangle comparison with a modulation index of $m = 30\,\%$, the gate signals are switched between -1 V and 16 V with a switching frequency of $f_{PWM} = 20.2$ kHz. The same models of the parasitic elements of the commutation cell, the same equivalent circuit of the DC-link capacitor and the same 3D geometry simulation to calculate the disturbance voltage at the LISN are used for all simulation results presented. The input data of the behavioral MOSFET model pictured in Figure 2 is varied to investigate the sensitivity of its parameters. The data measured is used initially to parameterize the MOSFET model. Figure 8 shows the simulation result for the load currents and the drain-source voltage of the low-side MOSFET of half-bridge W over one load cycle. The transient simulation result is compared with the measurements only in the time interval highlighted in Figure 8, because the rising and falling voltage-edge of V_{DS} changes with the drain-current.

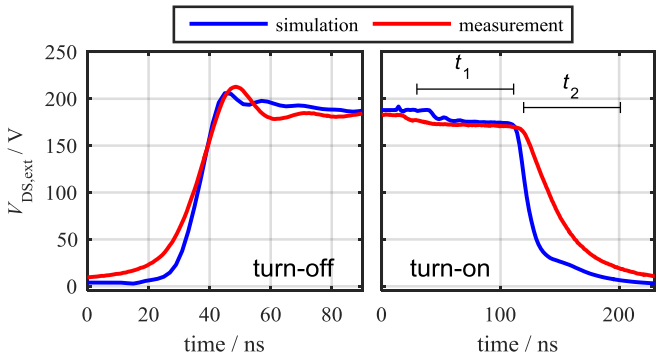

Fig. 9. Comparison of the time domain simulation result with measurements.

In this interval, Figure 9 compares the simulation results of $V_{DS,ext}$ with oscilloscope measurements from the real test setup. The simulation can reproduce the shape of the voltage curves for both the turn-on and the turn-off event, but the rise time and fall time are too small in both cases. Concerning the turn-off, the amount of overshoot is comparable to the measurements, but the frequency and the damping of the ringing deviates from the measurements. Further investigation showed that two dominant resonances cause this oscillation after turn-off. These resonances are marked as resonance *A* and *B* in Figure 10. *B* is caused by the commutation cell, where the output capacity C_{oss} of, for example, the

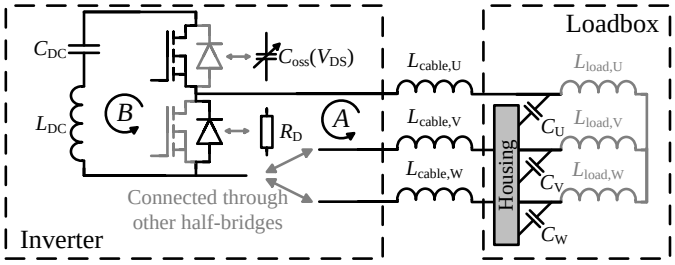

Fig. 10. Explanation for ringing occuring during turn-off events.

high-side MOSFET oscillates with the parasitic inductance L_{DC} of the DC-link capacitor and the busbar at approximately 70 MHz. *A* is caused mainly by the cables to the loadbox. Here, the inductivity of these cable together with the parasitic capacitances to the housing of the loadbox form a resonance circuit at approximately 5 MHz. Both frequencies can be retrieved in the spectrum of the disturbance voltage at the LISN (see Fig. 11). The investigations show that resonance *A* is well matched, but resonance *B* is shifted towards higher frequencies. This can be caused by two reasons: Either the

output capacitance C_{oss} is modeled too low or the parasitic inductance L_{DC} is modeled too high, which could be excluded by measurements using an impedance analyzer. The influence of the MOSFET capacitances on resonance *B* is investigated in section V.

Concerning turn-on, the voltage curve can be divided into the time intervals t_1 and t_2 (Fig. 9). The drain current rises during t_1, which causes a voltage drop over the inductances between drain and source before the drain-source voltage starts to fall during t_2. Both time intervals proceed too fast in the simulation and require further investigation. The deviations of the transient simulation cause an overestimation of the conducted EMI of the inverter. To investigate this, the V_{DS} of all MOSFETs of the inverter are converted into the frequency domain and used as excitations in a 3D geometry model in the form of ideal voltage sources to calculate the disturbance voltage at the LISN. Figure 11 compares the measured and simulated frequency spectrum of the disturbance voltage at the LISN in the frequency range of 0.3 to 110 MHz. The measurements are performed with a 12-bit oscilloscope for 1 ms and a sampling rate of 1 GS/s. A high-pass filter is used only for frequencies above 20 MHz to decrease the noise level. Subsequently, the time domain data measured are transformed into the frequency domain using a FFT algorithm. An envelope function is applied to the spectra for the sake of clarity. The simulation can reproduce the disturbance voltage up to 30 MHz precisely due to the detailed 3D geometry model. Above this frequency, the influence of the MOSFET model increases which leads to higher deviations between the simulation and the measurements.

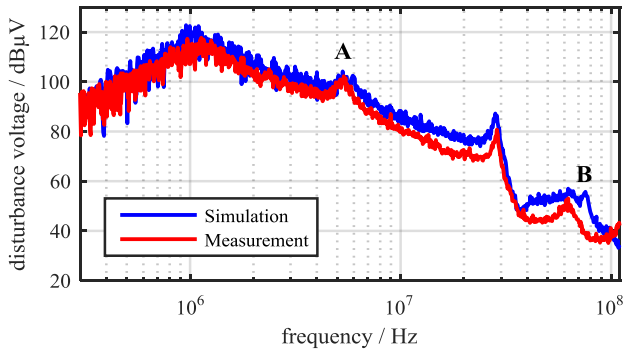

Fig. 11. Comparison between simulated and measured disturbance voltage.

IV. Variation of IV Curves

The input parameters of the MOSFET model are varied to investigate the root cause of this deviation. Starting with the IV curves of the MOSFET, three different variations are determined and pictured in Figure 12 at V_{GS} = 10 V. For IV_I, the functions of the IV curves are elevated only in the saturation region by increasing the threshold voltage V_{th} from 5.5 V to 6 V. The slope of the IV curves in the saturation region is constantly zero. This is modified for IV_{II} by defining an early voltage of V_{early} = -500 V, which creates a positive slope in this region as a function of the gate voltage. Finally, IV_{III} shows the influence of the linear region by reducing the $R_{DS,on}$ by the slope of this region without changing the saturation region.

Figure 13 compares the time domain simulation results of the different IV curves to each other. In summary, the saturation region shows a strong impact on the simulated switching behavior of the MOSFET. By contrast, the influence of the linear region seems to be low. Going into detail, it can be observed that lower IV curves in the saturation region lead to significantly slower switching times only of the turn-on event if the saturation region is modeled as flat. Adding a slope to the curves influences the turn-on and the turn-off event by reducing the slew rate in both cases.

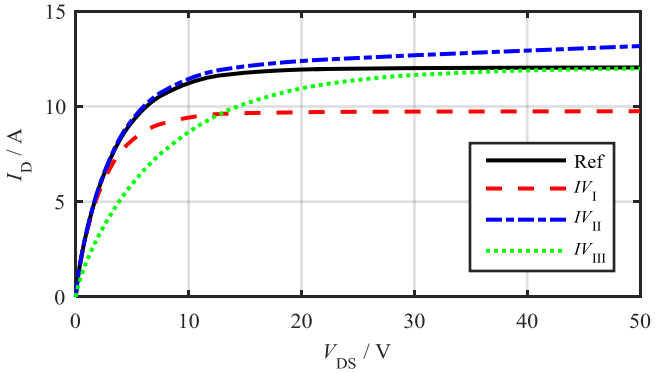

Fig. 12. Variation of IV curves of the MOSFET shown at V_{GS} = 10 V.

To explain the voltage curve during turn-off, it needs to be considered that V_{DS} depends only on the gate current and the drain-gate capacitance C_{GD}, as long as the slope of the IV curves is obtained as zero in the saturation region. Lower values of V_{th} or a lower slope of the transfer characteristic of the MOSFET initiate the turn-off at a higher gate-source voltage V_{GS} and, thereby, at a higher gate current. The effect can be seen in an earlier and slightly faster increase of the drain-source voltage V_{DS} (see variation IV_I). As soon as the slope of the IV curves is positive in the saturation region, the voltage curve depends not only on these parameters, but also on the gate-voltage V_{GS}. The gate-source capacitance C_{GS} is orders of magnitude larger than the gate-drain capacitance C_{GD}. Therefore, the discharging of C_{GS} is much slower than the charging of C_{GD}, which slows down the slew rate of V_{DS} as soon as a positive slope of the IV curves is defined in the saturation area (see variation IV_{II}).

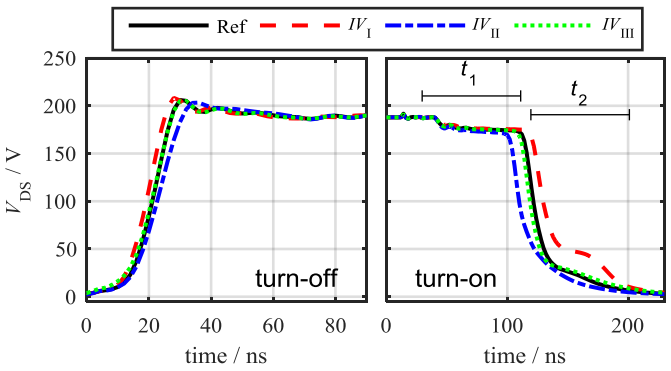

Fig. 13. Time domain simulation results for the variations of the IV curves.

Two different effects need to be distinguished for the explanation of the turn-on event. Firstly, it takes more time with lower values of V_{th} to achieve the gate voltage where the saturation current is equal to the load current. This time is equal to time interval t_1, where the voltage drop of the drain current is visible in V_{DS}. Secondly, with higher V_{GS} at the end

of this t_1, the gate current is lower, resulting in a faster discharging of C_{GD} and, thereby, a shorter fall time during t_2.

Applying the different time domain simulation results to the 3D geometry simulation shows the effect of the IV curves on the EMI of the inverter. Figure 14 compares the calculated frequency spectra of the disturbance voltage at the LISN of the IV curve variation presented in the frequency range above 10 MHz. The results show a slightly lower disturbance voltage for variation IV_{II} caused by the lower slew rates of V_{DS}, but the effect is too low to justify the deviations between the simulation and the measurement observed in Figure 11.

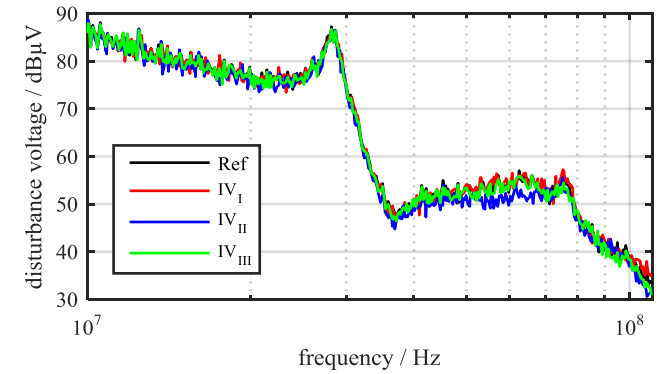

Fig. 14. Influence of the IV curves on the disturbance voltage at the LISN.

V. Variation of Voltage-Dependent Capacitances

The measurement of the semiconductor capacitances C_{GD}, C_{DS} and C_{GS} showed deviations, especially between the value of C_{GD} measured and the datasheet value. Consequently, the influence of this capacitance on the switching behavior and on the disturbance voltage at the LISN is investigated. Therefore, three different variations of the gate-drain capacitance are determined and compared in Figure 15 as a function of the drain-source voltage.

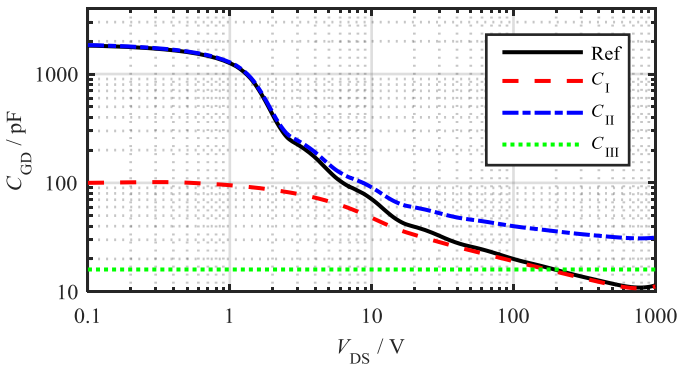

Fig. 15. Comparison of the voltage-dependent space-charge capacitances.

The measurements of the gate-drain capacitance show a strongly decreased value of C_{GD} for negative gate-source voltages V_{GS}, especially when V_{DS} is smaller than 10 V. This phenomenon is investigated with variation C_I using the capacitance measured at V_{GS} = -6 V. With variation C_{II}, an offset or calibration failure of the capacity measurement device is investigated. Therefore, a fixed capacity of 20 pF is added to C_{GD}, corresponding to the difference between the measurement and the datasheet displayed in Figure 3. Finally, C_{III} determines whether the capacitances generally need to be defined as a function of the drain-source voltage or if a fixed capacitor is sufficient. Therefore, a fixed capacity of $C_{GD}(V_{DC}) = C_{GD}(180\ \text{V}) = 16$ pF is used. A spline with 10 logarithmically distributed nodes is fitted to the capacity data and applied to the current source I_C (see Fig. 2) to get a flexible and practicable implementation of the capacitor.

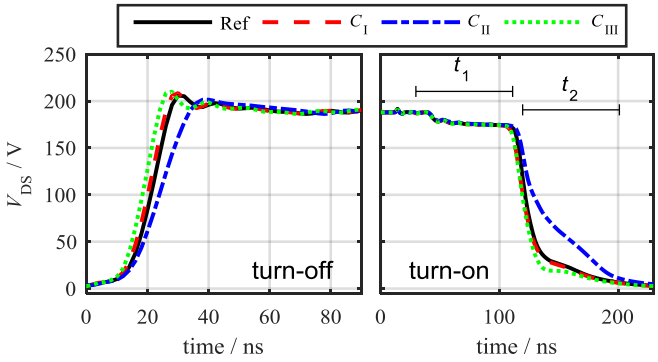

Fig. 16. Time domain simulation results for the capacity variations.

Figure 16 shows the time domain simulation results for the variation of the gate-drain capacitance. The results show a strong influence of this parameter on the switching behavior of the device. Higher values of C_{GD} correlate directly with the slower rise and fall time of V_{DS} during turn-on and turn-off. This can be explained by the charging time of this capacitance, which is equal to the rise time of V_{DS} during the entire turn-off and to the fall time of V_{DS} during time interval t_2. A higher capacity causes a longer charging time and, thereby, a lower slew rate of V_{DS}. Figure 16 shows the result of the disturbance voltage at the LISN, calculated from the time domain results with the help of the 3D geometry simulation It shows that a measurement error of only 20 pF can cause an EMI simulation error of 10 dB above 20 MHz. A much larger difference between the static and transient transistor capacitances of a comparable device is reported in [7]. Hence, this is a plausible reason for the deviation observed in Figure 11. The method shown in [7] can be used to improve the accuracy of the EMI simulation.

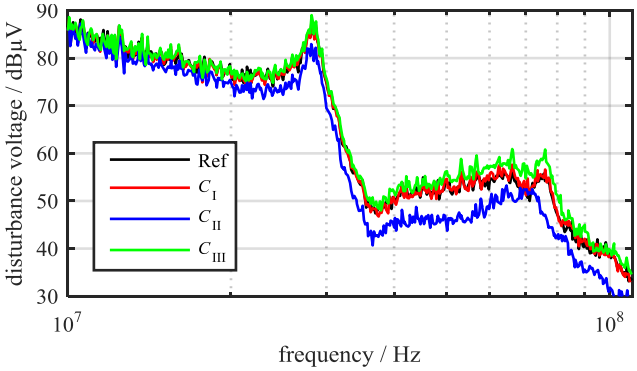

Fig. 17. Comparison of the voltage-dependent space-charge capacitances.

VI. Variation of the Diode and the Gate Resistance

The remaining two parameters of the model according to the EMI of the inverter are investigated with the variations described in Table 1 for the sake of a comprehensive sensitivity analysis. Instead of using a spline function fitted to the measured output characteristic of the diode, the model is

simplified for variation D_I and D_{II} by using an ideal diode with a forward voltage $V_{f,diode}$ and a single resistance $R_{ser,diode}$ connected in series to emulate the static losses of the diode. D_I and D_{II} are used to investigate both the effect of the deviating diode losses between measurements and datasheet values, and the dependency of the forward voltage $V_{f,diode}$ on the gate-source voltage V_{GS}. R_I is used to estimate the possible measurement uncertainties of the internal gate resistance. A value of $R_G = 10\ \Omega$ is chosen initially based on the manufacturer's model and verified later by measurements.

Table 1: Variation of diode and internal gate resistance.

Variation	$V_{F,DIODE}$	$R_{ser,diode}$	R_G
D_I	1 V	1 mΩ	10 Ω
D_{II}	3 V	100 mΩ	10 Ω
R_I	$I_{SD}(V_{DS},V_{GS})$ equal to Ref		5 Ω

The simulation results of the variations described above are compared to each other in the time domain (Fig. 18) and the frequency domain (Fig. 19) concerning the disturbance voltage calculated at the LISN.

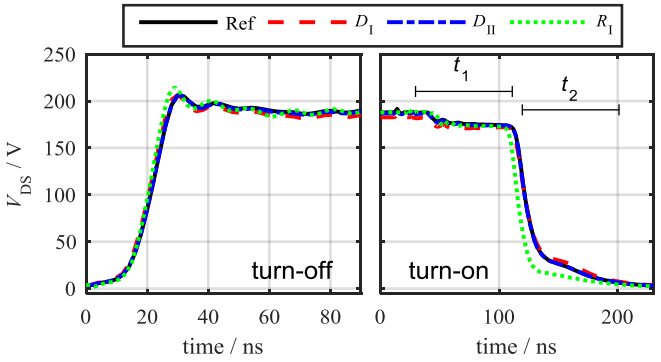

Fig. 18. Time domain simulation for the diode and gate resistance variations.

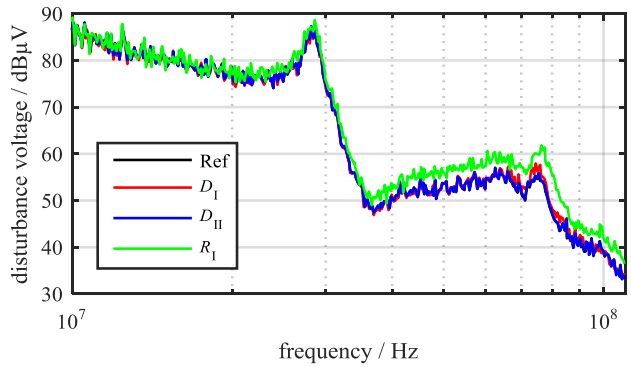

Fig. 19. AC simulation results for the diode and gate resistance variations.

Both results show the very low influence of the diode parameters on the switching behavior of the MOSFET in the time intervals investigated in Figure 18. The only relevant aspect for the EMI of the inverter is the damping of resonance *B*. Figure 19 shows a reduced disturbance voltage at that resonance for higher values of $V_{f,diode}$ and $R_{ser,diode}$. However, there are dynamic effects from the diode, such as the reverse recovery behavior, which cannot be investigated by the circuit presented. From a modeling perspective, the results encourage the simplification with an ideal diode and a series resistance which enables a reduced simulation time.

As expected, a decreased internal gate resistance R_G results in a faster turn-on and turn-off process, which is caused by the accelerated charging and discharging of the gate-source capacity C_{GS}. The internal gate resistance can generally be seen as an important parameter, but, in this case, the difference of 3 dB observed in Figure 19 shows a relatively low impact with respect to the strong variation of R_G, which is much larger than the measurement uncertainties expected.

VII. Conclusion and Outlook

This contribution uses a test setup similar to CISPR25 to investigate the influence of MOSFET parameters on the EMI of an automotive inverter. The analysis is carried out with a two-step simulation model. Firstly, a circuit simulation is presented which uses the parasitic elements of the commutation cell in combination with a MOSFET model presented to reproduce the transient switching behavior of the semiconductors. Subsequently, a 3D geometry simulation is used to calculate the disturbance voltage at the LISN based on the frequency spectra of the drain-source voltage of all MOSFETs. The simulation model reproduces the spectrum of the disturbance voltage at the LISN precisely up to 30 MHz. However, deviations up to 10 dB can be observed at higher frequencies.

Based on the simulation, a sensitivity analysis of the semiconductor capacitances, the IV curves of the MOSFET, the internal gate resistance and the diodes IV characteristic is performed. The results clearly identify the IV curves in the saturation region and the voltage-dependent capacitance between gate and drain of the MOSFET as the most relevant parameters regarding the EMI of the inverter. These data are not precisely accessible in most of the MOSFET datasheets and requires further investigations regarding the estimation of the IV curves at high drain currents and high drain-source voltages, as well as precise measurements of the gate-drain capacitance in an ON and OFF state of a MOSFET.

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