

Understanding Conducted Emissions from an Automotive Inverter Using a Common-Mode Model

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Abstract—This contribution presents results from an investigation on conducted emissions of an automotive inverter in a component level EMC test setup with unshielded cables. The primary goal of the investigation is to develop a profound understanding of the shape of the disturbance voltage's frequency spectrum at the line impedance stabilization network. Complying with that objective, common-mode currents are identified as the dominating noise currents especially in the operating point of the inverter representing the worst case scenario regarding EMC performance. To support this conclusion an AC simulation of a single phase common-mode equivalent circuit of the system is presented. The occurring resonances in the noise spectrum and its overall shape are explained by the simulation within the frequency range of 100 kHz to 110 MHz. In addition, C_Y capacitors are used as common-mode filter elements. Based on the validated simulation model the influence of the filter capacitors and their parasitic inductances are investigated.

Keywords—common-mode model; conducted emissions; traction inverter; inverter stray capacitances

I. INTRODUCTION

The electrification of the automotive drive train brings new challenges related to electromagnetic compatibility (EMC). A state of the art drive train of an electric vehicle consists of a high voltage (HV) battery, an inverter and an electric machine. To convert the battery DC voltage into a three-phase AC current, power semiconductors are used in the inverter. To increase the efficiency of the inverter fast switching times are needed however, they cause radio frequency (RF) spectral components with high amplitude [1]. These disturbances propagate through various coupling paths throughout the drive train and can disturb other electric devices like sensors and

mobile communication. Therefore EMC engineering is fundamental not only to ensure the security of the occupants but also to establish the comfort inside the vehicle for example in form of uninterrupted communication. According to CISPR 25 [2] the disturbance voltage at the line impedance stabilization network (LISN) can be measured with an electromagnetic interference (EMI) test receiver to characterize the drive train components concerning their EMC behavior. The prediction of the EMC performance of a component of the electric drive train is important for car and component manufacturers because an early estimation of the occurring emissions is directly related to cost reduction [3]. Therefore, a good estimation of the disturbance voltage at the LISN and a profound knowledge about all influencing effects is desirable.

To investigate the conducted emissions of the inverter, this contribution presents a test setup similar to CISPR 25 which is shown in Fig. 1. The setup consists of two connected LISNs to emulate the high frequency behavior of the traction system (HV battery and cables), an automotive inverter and a symmetrical three-phase load (3~load). The three components are mounted on a conductive measurement table and connected to each other with unshielded cables. The disturbance voltages at the LISN V_{HV+} and V_{HV-} are caused by common-mode (CM) and differential-mode (DM) currents [4]. Both currents are measured in the test setup during operation of the inverter. Subsequently, a profound knowledge about the excitation and propagation of the CM currents is developed. Therefore, a frequency domain CM simulation is performed. Based on the simulation results, the shape and the occurring resonances of the frequency spectrum of V_{HV+} and V_{HV-} can be explained by the resonant circuits in the simulation model.

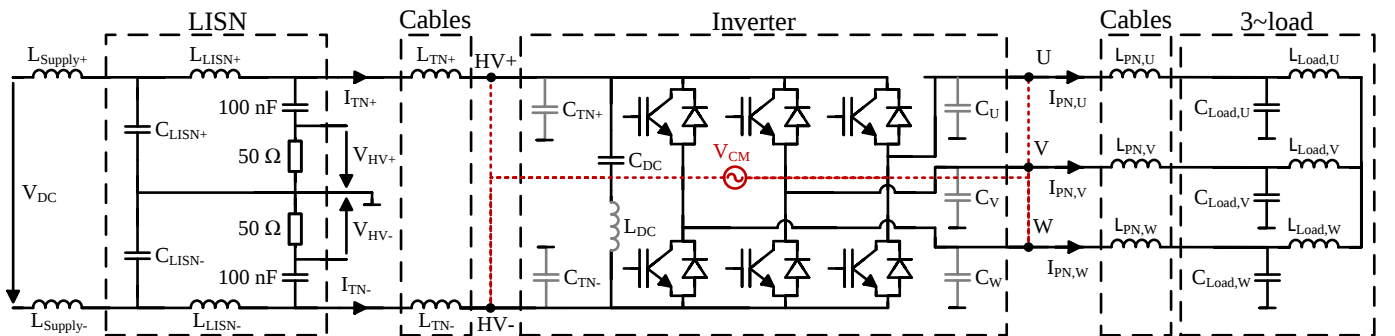


Fig. 1. Simplified equivalent circuit of test setup consisting of two LISNs, inverter and 3~load. Excitation of common-mode currents with sinusoidal voltage V_{CM} .

II. INVESTIGATED TEST SETUP

A. Control of Automotive Inverter

As shown in Fig. 1 the used inverter consists of six IGBTs (insulated gate bipolar transistor) where two are connected in a half bridge circuit. The resulting three half bridges can be used to connect HV+ or HV- to U, V and W individually. To control the power electronic switches of the half bridges a control algorithm based on a sine-triangle comparison is used [5]. The basic principle of the algorithm is shown in Fig. 2.

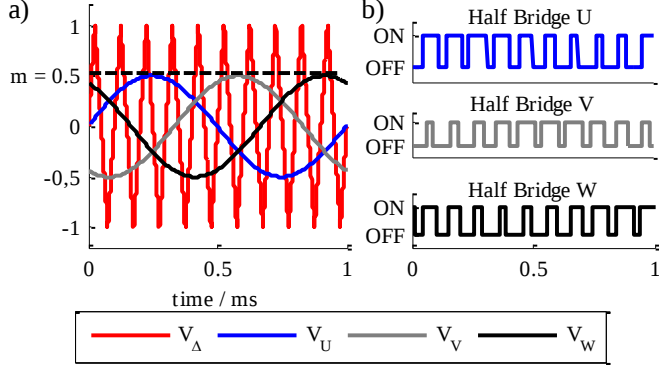


Fig. 2. a) Carrier and reference signal used for the sine-triangle comparison. b) Resulting control signals for halfbridges U, V and W of the inverter.

The carrier signal V_Δ is a periodical triangle function with a frequency of $f_{PWM} = 10.2$ kHz. For each half bridge a 1 kHz sinusoidal reference signal is defined (V_U , V_V and V_W). The relation of the maximum amplitude of the carrier and the reference signal is given by the modulation-degree m which is set to 50% in Fig. 2. If a reference signal exceeds V_Δ the high-side switch of the associated half bridge is closed and the low-side switch is opened. Otherwise, the switches are opened and closed vice versa. During switchover a blanking-time of $1.6 \mu s$ avoids short circuits.

For all following measurements and simulations V_{DC} is set to 250 V. With the control algorithm presented in Fig. 2 the load currents have a sinusoidal waveform, 120° phase shifted to each other with a frequency of 1 kHz, an amplitude of 70 A.

B. Influence of Control Algorithm

During operation of the inverter, the disturbance voltage V_{HV+} at the LISN is measured with an EMI test receiver according to CISPR 25. For all measured frequency spectra the average detector is used inside the EMI test receiver. In contrast to the standard, the internal filter bandwidth (IFBW)

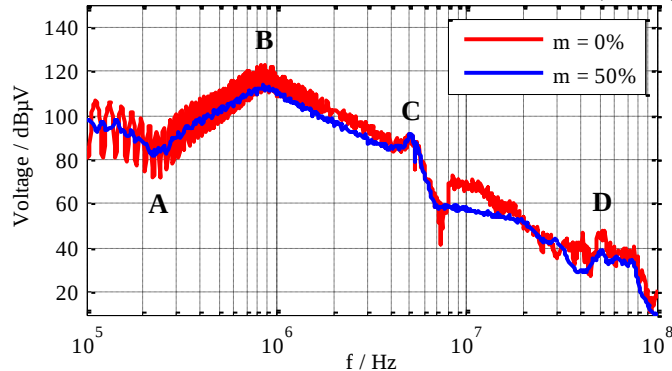


Fig. 3. Average frequency spectrum of V_{HV+} measured at LISN during operation of the inverter with a modulation degree of 0% and 50%.

of the EMI test receiver is set to 9 kHz for the entire frequency range between 100 kHz and 110 MHz to avoid voltage steps caused by changes of the IFBW. Fig. 3 shows the frequency spectrum of the disturbance voltage V_{HV+} at the LISN using the control algorithm described in chapter II-A. If m is set to 0 %, the three reference signals are equal to zero and the three half bridges are switched simultaneously on and off with the frequency f_{PWM} and a duty-cycle of 50 %. By means of the Fourier series this periodical rectangular signal f_{rect} can be transformed into frequency domain [6].

$$f_{rect}(t) = \frac{4V_{DC}}{\pi} \sum_{k=1}^{\infty} \frac{\sin(2k-1)\omega t}{2k-1} \quad \text{with } \omega = 2\pi f_{PWM} \quad (1)$$

According to (1) the equation the excitation has spectral components at odd multiple of the carrier signal's frequency. Because the IFBW of the EMI test receiver considers a frequency range at one measurement point, this results in local maxima of the spectrum at an interval of $2f_{PWM} = 20.4$ kHz. The position of the maxima will change within one period of the reference signal if m is greater than zero. Due to the average detector and a measurement time greater than the period of the reference signals, those local maxima disappear when m is increased. Concerning a maximum disturbance voltage Fig. 3 shows that m equal zero can be regarded as worst case of the possible modulation degrees.

C. Common-Mode and Differential-Mode Currents

According to [4] the disturbance voltages V_{HV+} and V_{HV-} are caused by CM and DM currents. The origin of the CM currents is the falling and rising edge of the voltage between HV+/- and U, V and W respectively. The DM currents mainly come from the voltage ripple across the DC-link capacitor C_{DC} and its parasitic inductivity L_{DC} . For the traction side (DC voltage side) of the inverter I_{CM} and I_{DM} can be calculated with (2) and (3).

$$I_{CM} = I_{TN+} + I_{TN-} \quad (2)$$

$$I_{DM} = I_{TN+} - I_{TN-} \quad (3)$$

Fig. 4 shows the frequency spectrum of I_{CM} and I_{DM} during operation of the inverter with $m = 0$ % measured with a F65 (Fischer Inc.) current clamp.

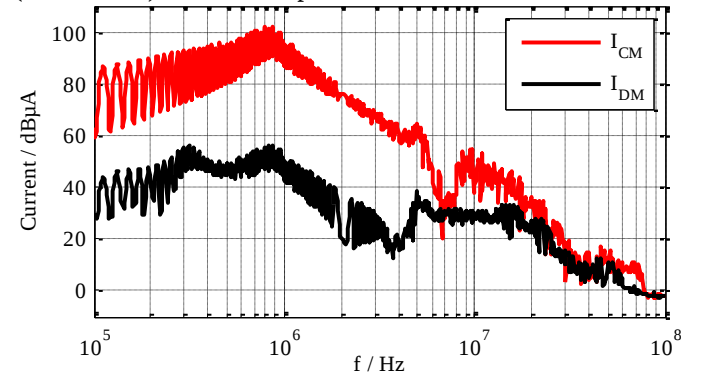


Fig. 4. Average frequency spectrum of I_{CM} and I_{DM} at $m = 0\%$.

Neglecting the resonance frequency at 7 and 30 MHz, I_{CM} is higher than I_{DM} in the complete frequency range. Below 20 MHz the difference between the two currents is constantly higher than 6 dB. Towards higher frequencies, this distance decreases. The CM currents can be identified as the

dominating noise currents at this operating point of the inverter. Based on this conclusion, the excitation and propagation of CM emissions are investigated. To understand the overall shape of the disturbance voltage frequency spectrum V_{HV+} shown in Fig. 3, a CM simulation model is developed to explain the resonances A to D.

D. Simulation Model

All presented simulations in this contribution are performed in frequency domain using a SPICE solver. Neglecting the nonlinear effects of a circuit, the simulation time in frequency domain depends on the number of frequency points and is therefore less time consuming than the simulation in time domain. In contrast to other publications, this contribution focuses more on the simplicity of the model rather than on an exact calculation of the noise voltage. After reducing the number of elements of the equivalent circuit to a minimum, a parameter variation of the main system variables easily shows the impact of each element on the noise spectrum.

The basic principle of the used CM simulation model is a single CM voltage source marked in Fig. 1. Starting from the model presented in [7] HV- and HV+ as well as U, V and W respectively are short circuited in the model. One can justify this approach on both sides of the inverter. On the traction side, the parasitic inductance L_{DC} of the used DC-link capacitor C_{DC} has a value of 15 nH and an impedance of less than 10 Ω at 100 MHz. This is close to a short circuit compared to the impedances of the other components. On the phase side U, V and W are connected simultaneously to HV- or HV+. Therefore, they are connected with each other due to the control algorithm and the chosen operating point with $m = 0\%$. For a plausibility check, the tree points are short circuited externally. The measured deviation of the disturbance spectrum V_{HV+} with and without external short circuit is less than 1 dB for the complete frequency range.

In the simulation model, the CM excitation V_{CM} is located between the two resulting potentials of the traction and phase side of the inverter. Because the remaining parts of the test setup are symmetrical, the two LISN, the 3~load and the cables are combined to the single phase equivalent circuit shown in Fig. 5.

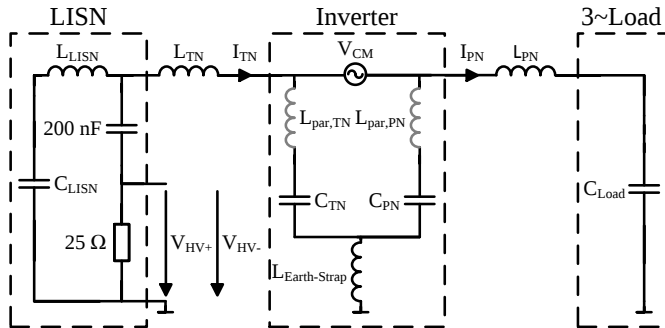


Fig. 5. Equivalent circuit of a single phase CM simulation.

The cables on both sides of the inverter are replaced by L_{TN} and L_{PN} representing the cables of Fig. 1 connected in parallel. (L_{PN} and L_{TN} are measured with an impedance analyzer). The description of the remaining components of the equivalent circuit is divided into two parts. The first part is the spectrum

of the excitation V_{CM} and the second part is the transmission path from the disturbance source to the LISN which includes the impedance characterization of the LISNs, the inverter and the load.

III. COMMON-MODE EXCITATION AND COUPLING PATH

A. Excitation – Frequency Components of Switching Edge

Considering the noise currents as CM currents, the rising and falling edge of the potentials at U, V and W referred to HV+ and HV- can be determined as the disturbance source. Exemplarily the time domain signal of the voltage between U and HV- during switch on of the corresponding half bridge is shown in the small graph in Fig. 6. Based on the measured pulse, the rise time can be estimated with $\tau = 100$ ns.

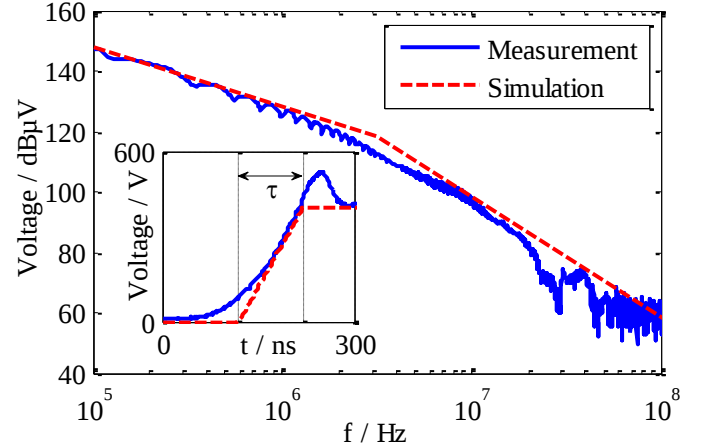


Fig. 6. Comparison of switch on pulse in time and frequency domain of measurement and simulation with $f_{PWM} = 10.2$ kHz and duty cycle $d = 50\%$.

The main graph in Fig. 6 shows a comparison in frequency domain. Using the same PWM pulse with a period time of $T = 100 \mu s$ and a duty cycle of $d = 50\%$, the blue curve is the Fourier transformation of the measured time domain signal and the red curve the analytical calculation of the envelope based on an ideal trapezoidal pulse. Considering the aim of the investigation, the approximation of the excitation with the analytic envelope can be taken as sufficient. The envelope's two corner frequencies f_1 and f_2 are given by (4) and (5) [6].

$$f_1 = \frac{1}{\pi T} = \frac{1}{\pi \cdot 100 \mu s \cdot d} = 6.37 \text{ kHz} \quad (4)$$

$$f_2 = \frac{1}{\pi \tau} = \frac{1}{\pi \cdot 100 ns} = 3.18 \text{ MHz} \quad (5)$$

According to (4) f_1 is lower than 100 kHz if the duty cycle is greater than 3.18% (guaranteed due to the blanking-time). Above this value f_1 is outside the measured frequency range. The value of the envelope at f_2 is given by (6) if the switch-on time is greater than the rise time [6].

$$V(f_2) \cdot \frac{1 dB \mu V}{1 V} = 20 \cdot \log \left(\frac{2 \cdot V_{DC} \cdot \tau}{T \cdot 1 \mu V} \right) \quad (6)$$

Equation (6) shows the independence of the envelope's shape of the duty cycle in the investigated frequency range. As a consequence, it is sufficient to investigate the worst case scenario with $m = 0\%$.

B. CM Impedances of LISNs, Inverter and Load

1) LISN

Special HV-LISNs, designed according to [8], are available on the market to emulate the characteristic impedance of a HV traction system. The difference between the conventional LV-LISNs and the HV-LISNs is the capacity to ground which is called C_{LISN+} and C_{LISN-} in Fig. 1. Hereby, 100 nF are used in the HV-LISN and 1 μ F in the LV-LISN. Fig. 7 shows a comparison between the measured spectrum of V_{HV+} using two LV- or two HV-LISNs.

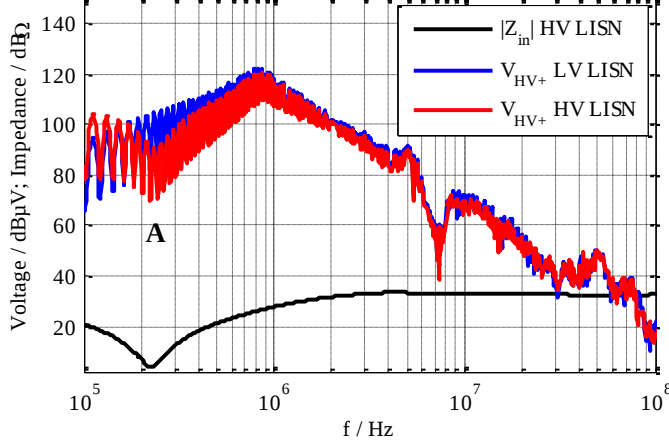


Fig. 7. Frequency spectrum of V_{HV+} measured using a HV-LISN or a LV-LISN compared to the input impedance of a HV-LISN.

The impedance Z_{in} of the HV-LISN plotted in Fig. 7 explains the local minimum A at 230 kHz of V_{HV+} which is caused by the resonance frequency of L_{LISN+} (5 μ H) and C_{LISN+} (100 nF). Using the LV-LISNs, this resonance frequency occurs at 23 kHz outside the measured frequency range.

For the single phase equivalent circuit of Fig. 5 two HV-LISNs are connected in parallel. Therefore, the value of the capacitances is doubled and the value of the inductances is cut in half. The calculated resonance frequency does not change. The disturbance voltages V_{HV+} and V_{HV-} are now equal to each other and measured over a common 25 Ω resistance because both 50 Ω resistances are connected in parallel.

2) Inverter

In the test setup, the inverter's heat sink is connected to the measurement table with a 10 cm copper strap. For the simulation the inductance $L_{Earth-Strap}$ of this copper strap is estimated with 10 nH. $HV+$, $HV-$ as well as U, V and W are isolated from the heat sink. However, there is a parasitic capacitance between each of this five points and the cooling plate, mainly caused by the stray capacities of the power semiconductor module. For the single phase equivalent circuit those capacitances are combined to one capacitor at each side of the inverter. The resulting capacitances C_{TN} and C_{PN} can be measured with a vector network analyzer (VNA) using two ports. Therefore, both sides of the inverter are short circuited to each other. Port 1 is connected to $HV+/HV-$ and Port 2 to U/V/W, both referred to the heat sink (see Fig. 8). Referring both ports to this point allows the usage of very small adapters with very low influence on the measurement result. To calculate the values of C_{TN} and C_{PN} the measured S-Parameter matrix can be transformed into the admittance matrix Y [9]. The impedances at and between the ports are given by (7)–(9).

$$Z_{C_{TN}} = \frac{1}{Y_{11} + Y_{12}} \quad (7); \quad Z_{12} = \frac{1}{-Y_{12}} \quad (8); \quad Z_{C_{PN}} = \frac{1}{Y_{22} + Y_{21}} \quad (9)$$

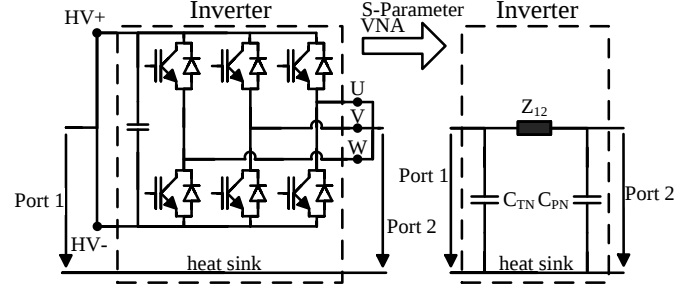


Fig. 8. Measurement principle to calculate the parasitic capacitance to the heat sink on both sides of the inverter and the impedances of the switches.

This method allows the measurement of the stray capacitances C_{TN} and C_{PN} separately. For the used inverter the main part of these capacitances is located inside the semiconductor module. Concerning a plate capacitor model the measured capacitances correlate very well with the size of the surface layer inside the IGBT module. For higher frequencies the impedances of these elements are inductive because of the length of the traces. This influence is considered by the inductances $L_{par,TN}$ and $L_{par,PN}$ in Fig. 5.

3) 3~Load

Because a real motor needs to be cooled and decelerated without affecting the EMC behavior of the test setup, there are various investigations such as [10] to emulate the high frequency behavior of the electric machine with a passive network. For simplicity reasons, the motor's stator impedances are replaced by three air-core coils ($L_{Load,U}$, $L_{Load,V}$ and $L_{Load,W}$) connected together to a neutral point. Additionally a capacitance to ground at each phase ($C_{Load,U}$, $C_{Load,V}$ and $C_{Load,W}$) emulates the parasitic capacity to the housing of the motor. This symmetrical load pictured in Fig. 1 is combined to one phase in Fig. 5. For CM currents only the three capacitances to ground are relevant, which are combined to C_{Load} . The three stator inductances can be neglected.

IV. RESULTS OF SINGLE PHASE AC-SIMULATION

Fig. 9 shows the simulation result of the AC-simulation based on the equivalent circuit of Fig. 5. The voltage source V_{CM} creates a spectrum according to the approximation with the analytic envelope of Fig. 6. As the result shows, the overall shape of the disturbance voltage frequency spectrum and its resonances can be reproduced well by the simulation.

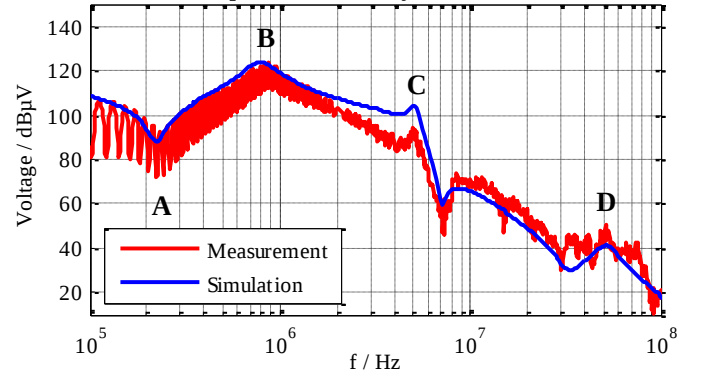


Fig. 9. Comparison between disturbance voltage spectrum measured with a EMI test receiver and simulation results from single phase CM simulation.

A. Evaluation of Resonances of the Noise Spectrum

Based on the simulation results, the remaining resonances B to D are explained in the following. Due to the fact that none of the three resonances can be allocated in the analytic envelope of the excitation source V_{CM} the shape of the disturbance voltage spectrum has to be caused by the CM impedance network of the test setup. Therefore one series or parallel resonant circuit for each of the resonances B-D is presented.

1) System Resonance B

To understand the resonance B the equivalent circuit of the CM model is simplified to the relevant elements in Fig. 10. The ideal voltage source V_{CM} is replaced by a short circuit.

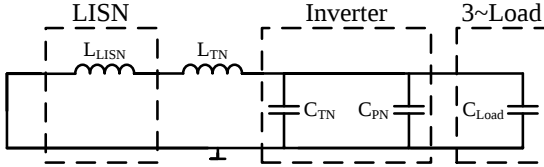


Fig. 10. Equivalent circuit explaining the system resonance B at ~800 kHz.

The simplification results in a series-resonant circuit consisting of the inductances of the LISNs and the cables on the traction side of the inverter and the parasitic capacitances of the inverter and the load. The impedance minimum of this circuit occurs at the resonance frequency f_B given by (10).

$$f_B = \frac{1}{2\pi\sqrt{(L_{LISN}+L_{TN}) \cdot (C_{TN}+C_{PN}+C_{Load})}} \quad (10)$$

At f_B , the CM current through the LISN reaches the maximum which leads to the maximum voltage drop over the 25 Ω resistance.

2) Inverter-Load Resonance C

In analogous manner the CM equivalent circuit is reduced to the relevant elements for the resonance C in Fig. 11-a).

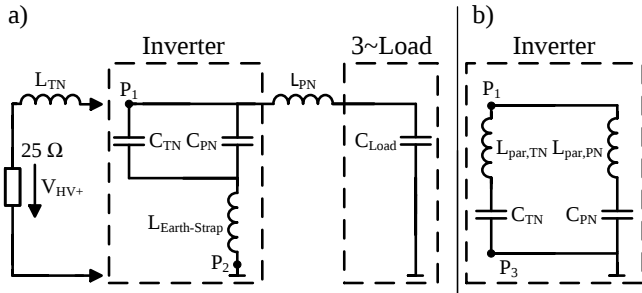


Fig. 11. a) Equivalent circuit explaining inverter load resonance C at ~5 MHz. b) Equivalent circuit explaining the inverter resonance D at ~50 MHz.

Resonance C is described as the inverter-load resonance because the inverter and the 3~load form a resonance circuit with minimum impedance at f_C given in (11).

$$f_C = \frac{1}{2\pi\sqrt{(L_{Earth-Strap}+L_{PN}) \cdot \frac{(C_{TN}+C_{PN}) \cdot C_{Load}}{C_{TN}+C_{PN}+C_{Load}}}} \quad (11)$$

There is a local maximum of the voltage drop between P1 and P2 at f_C . Neglecting the series capacity of 100 nF inside the LISN, L_{TN} and the 25 Ω resistance are connected in parallel to these two points and form a lowpass filter for the disturbance voltage. This leads together with the resonance circuit to the local maximum C of the disturbance voltage in Fig. 9. The deviation between the simulated and measured

disturbance voltage at C is caused by the low correlation between the real excitation and the analytic envelope at that frequency.

3) Inverter resonance D

The inverter itself forms a resonance with the parasitic capacitances to the heat sink and the corresponding parasitic inductances; see Fig. 11-b). The resonance frequency of the associated circuit is given by (12).

$$f_D = \frac{1}{2\pi\sqrt{(L_{par,TN}+L_{par,PN}) \cdot \frac{C_{TN} \cdot C_{PN}}{C_{TN}+C_{PN}}}} \quad (12)$$

The lowpass filter of L_{TN} and the measurement resistance is extended with the inductance of the earth strap and causes the local maximum D of the disturbance voltage when the voltage drop between P1 and P3 reaches its maximum.

V. INFLUENCE OF C_Y CAPACITORS

In the next step, the test setup is extended with CM filters using C_Y capacitors. Assembled in parallel to the parasitic capacitances C_{TN+} and C_{TN-} , C_Y capacitors create a low impedance path for CM disturbances at the DC side of the inverter to ground. Due to this bypass the noise currents flowing through the LISNs and their resulting disturbance voltages are reduced. However, real C_Y capacitors have a non-ideal electrical behavior. Caused by the parasitic inductance of the built in capacities the positive effect of the filter on the noise spectrum is limited to a certain maximum frequency. The inductance is caused by two reasons. First, the internal inductance of the capacitor itself and second the interconnection technology to the housing of the inverter. In Fig. 12 the effect of the inductance on the noise spectrum is shown. For the investigation the same pair of capacitors is used in three different configurations. For configuration 1 only the capacitors are used. For configuration 2 and 3 air coil chokes with 28 nH and 47 nH respectively are added in series to the capacitor to simulate an increased parasitic inductance.

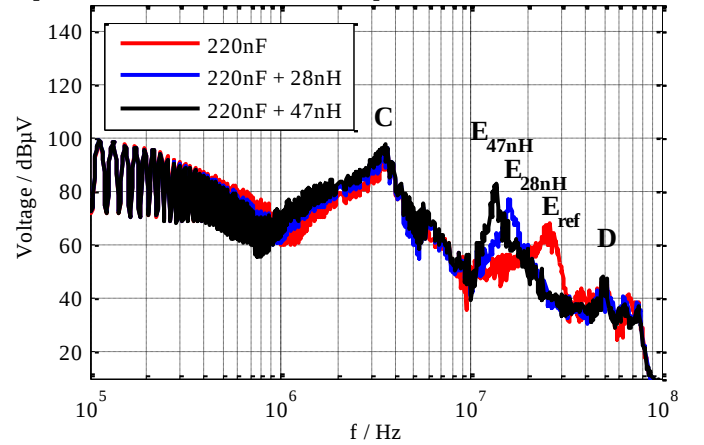


Fig. 12. Measured influence of C_Y 's parasitic inductivity on disturbance voltage frequency spectrum V_{HV+} .

The results show a decreased noise spectrum in all of the three configurations compared to the setup without C_Y capacitors. At the resonance frequency of the C_Y capacitor at approximately 1 MHz the capacitive behavior of the filter turns into inductive behavior. Above this frequency three resonances C, E and D can be distinguished. The resonances C and D can be recognized as the inverter-load resonance (C)

and the inverter resonance (D). Both resonances are shifted towards lower frequencies because the filter capacity enlarges the capacity of the inverter on the traction side. To understand the resonance E both C_Y capacitors are added to the CM equivalent circuit as the capacitor C_Y with its parasitic inductance L_{CY} . Fig. 13 shows the resulting equivalent circuit.

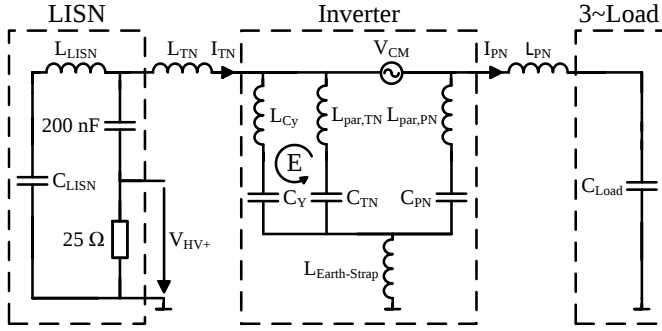


Fig. 13. Equivalent common-mode circuit extended with C_Y filter capacitor.

Based on the extended circuit the CM simulation is performed in analogous manner to IV. The simulation result of the disturbance voltage V_{HV+} for the variation of L_{CY} is shown in Fig. 14. Still, the simulation can reproduce the effect of the C_Y filter capacitors and its inductance.

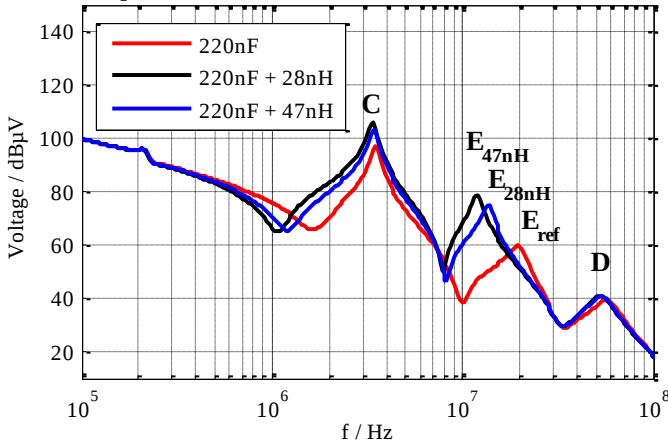


Fig. 14. Simulated influence of C_Y 's parasitic inductivity on disturbance voltage frequency spectrum V_{HV+} .

Subsequently, a parameter study of the elements used in the equivalent circuit shows, that resonance E is mainly influenced by C_Y , L_{CY} and the parasitic capacitances of the inverter C_{TN} and C_{PN} . These elements form a resonance circuit which is marked in Fig. 13. For the investigated test setup L_{CY} is much larger than $L_{par,TN}$ and $L_{par,PN}$. At resonance E, the impedance of the parasitic inductances on the traction and phase side of the inverter are small compared to the parasitic inductance of the filter. Therefore, C_{TN} and C_{PN} can be regarded as connected in parallel. To calculate the frequency of resonance E, the two capacities need to be summarized. Due to the fact, that C_Y is much larger than C_{TN} and C_{PN} , the resonance frequency is mainly influenced by the inverter's parasitic capacities and the parasitic inductance of the filter.

The simulation and measurement results of the disturbance voltage with filter capacitors show that the noise voltage can be reduced for low frequencies. The negative effect of the filter is an additional local maximum of the disturbance

voltage frequency spectrum which can be decreased and shifted towards higher frequencies when the parasitic inductance of the filter capacitors is minimized.

VI. CONCLUSION AND OUTLOOK

To investigate the EMC performance of an automotive inverter, a test setup similar to CISPR 25 is presented. For this setup, CM currents are identified as the dominating noise currents, especially for a modulation degree of $m = 0\%$ which represents the worst case scenario of the control algorithm concerning EMC performance.

A simple single phase CM AC simulation model is presented which can reproduce the shape of the disturbance voltage's frequency spectrum very well even when C_Y filter capacitors are added to the inverter. With the help of this entirely described model each of the occurring resonances in the spectrum can be explained with an according parallel or series resonant circuit of the CM impedance network.

Inside the inverter, the parasitic capacities and inductances between the ports of the inverter and the heat-sink mainly influence the disturbance voltage at the LISN. A VNA measurement method is presented to measure the absolute value of the stray capacities on both sides of the inverter separately. The parasitic inductances as well as the location of the parasitic elements cannot be determined with this method. With the help of 3D field simulation software these elements will be investigated in future work.

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