Derating of Ceramic Capacitors under ESD Stress

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***Abstract*—This paper considers the derating of common 0603-sized capacitors during electrostatic discharges from a human body model network. The derating of ceramic capacitors is generated by applying multiple electrostatic discharges with steadily increasing the charging voltage of the ESD gun. The electric characteristic data are measured during this process continuously.**

***Keywords*—Electromagnetic Compatibility, EMC, Electrostatic Discharge, ESD, Human Body Model, HBM, Ceramic Capacitor, Capacitance, Resonance Frequency**

I. Introduction

The electromagnetic compatibility (EMC) of electronic control units can be improved using ceramic capacitors. These capacitors cause a low-pass characteristic on the line they are protecting, effectively improving the electromagnetic compatibility of the device by reducing the conducted emissions from this line as well as increasing the electromagnetic immunity towards conducted interference travelling over the wiring into the device.

Electronic control units are generally interfaced to a wire or wiring harness using a multipoint connector. During the so called packaging and handling procedures the units and especially their connector pins are potentially exposed to electrostatic discharges originating from manufacturing or repairing personnel, their tools or machinery.

This paper introduces the measurement setup as well as first results concerning the derating effects of electrostatic discharges (ESD) on ceramic capacitors.

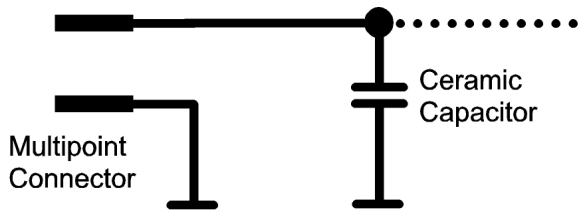

Figure 1. Simplified input circuit diagram of an arbitrary electronic control unit providing a decoupling capacitor directly after the multipoint connector interface.

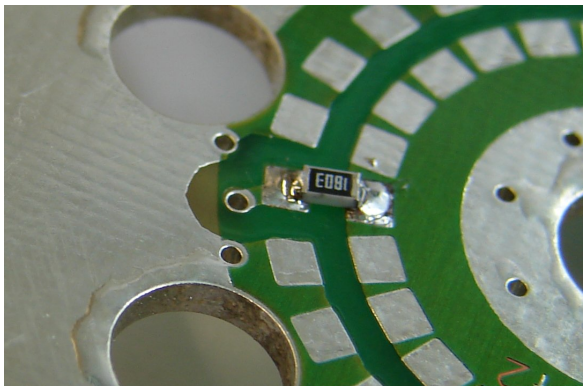

Figure 2. Single surface mounted device soldered to the Pommerenke target PCB. The picture shows the PCB not being integrated into the Pommerenke target.

II. Measuring Setup

The setup provides a single capacitor with a worst-case human body model (HBM) ESD stress from a 150pF/330Ω discharge network. Any circuitry connected to the capacitor under test and normally encountered in a real-world electronic control unit is left out intentionally. Worst-case conditions concerning ESD are achieved by a mechanically small, electrically low-inductive and low-resistant measurement setup.

The setup therefore mainly consists of a Pommerenke ESD target which adapts the capacitor under test (CUT) to the ESD simulator in a close to standard manner. ”Close to standard” here refers to the standard setup and equipment used for confirming the impulse shape of an ESD simulator to comply with, e.g. ISO 10605. Normally, a Pommerenke target, as well as it’s predecessor, the Pellegrini target, is made of an array of electrically parallel resistors which are mounted in a coaxial manner around the discharge point. This common current shunt design rule provides a geometrically symmetrical current distribution and thereby prevents magnetic coupling. Since the design of the Pellegrini target depends on the mechanical properties of the resistor array, it is not easy to adapt this target type to be used for measuring a single component, here a single SMD capacitor (Fig. 2).

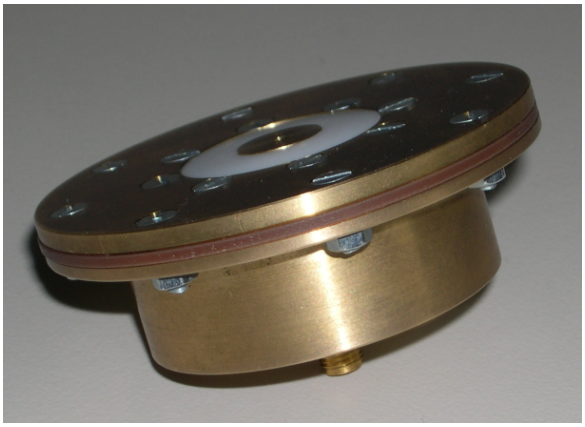

Figure 3. Pommerenke target with integrated PCB. The PCB between the brass material is mounted with the CUT (not visible). The centre electrode surrounded by the white material on the top plane is contacted with the ESD Simulator Gun Tip during ESD Stresses.

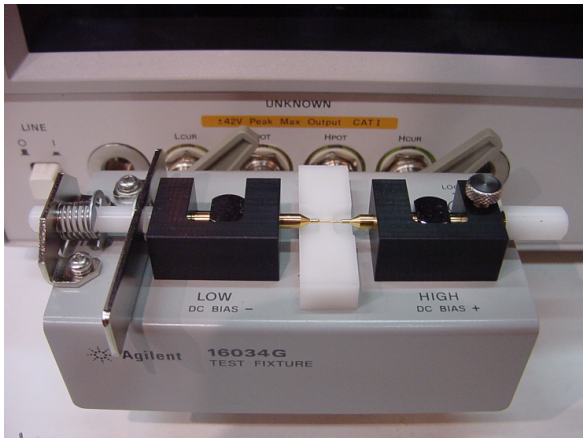

Figure 4. Fixture of the impedance analyser for measuring SMD components. The CUT is inserted between the golden tips in the middle of the fixture during measurement.

Especially, since the CUTs would not be easily dismountable in case of the Pellegrini target, the choice was made to use the Pommerenke ESD target design (Fig. 3) as the basis of the measurement setup of the investigations presented here.

In summary, the Pommerenke target design features several advantages over the Pellegrini target design:

1) Accessibility of the CUT
2) Inherent support for surface mounted devices
3) Higher bandwidth due to smaller dimensions
4) Better mechanical reproducability because of simpler design

The printed circuit board of the Pommerenke target is mounted exclusively with the CUT, which remains in the target while being stressed, discharged and measured before being stressed again.

Since the CUT has to be taken out of the ESD target after being stressed and discharged in order to be measured (see next section for details), the target was enhanced with a solder-free fixture. This way the CUT can be integrated and removed from the ESD target without going through the time consuming effort of the manual precision soldering.

During the ESD stress the target with the CUT is integrated into the centre of a vertical coupling plane sized 0.5 m x 0.5 m, as defined for the EN 61000-4-2 test setup. The vertical coupling plane is connected directly with the ground lead of the ESD simulator gun without using any bleed-off resistors.

III. ESD and Measuring Sequence

The test sequence starts with a zero voltage, or pre-stress measurement of the CUT's capacitance. This capacitance value will later be used for normalising the changed capacitance values measured in the progress of the derating process.

The whole ESD and measuring sequence can be divided in two main steps:

1) Measuring step - measuring the small signal characteristics of the CUT
2) Stressing step - stressing the CUT with multiple ESD impulses, each followed by discharging the CUT

This sequence is repeated continuously, while increasing the stress voltage level after every measuring step until the last stress voltage level is reached.

For measuring the small signal characteristics the CUT is inserted into a SMD fixture attached to an impedance analyser (Fig. 4). This equipment is configured to read out the capacitance of the CUT over a frequency range from 40 Hz to 110 MHz. After performing this measuring step, the CUT is taken back to the enhanced Pommerenke target for further stressing.

The stress voltage levels applied to the CUTs during the single ESD stressing steps presented here were defined as follows:

1) +/- 0.5 kV
2) +/- 1.0 kV
3) +/- 1.5 kV
4) +/- 2.0 kV
5) +/- 2.5 kV
6) +/- 3.0 kV
7) +/- 3.5 kV
8) +/- 4.0 kV
9) +/- 4.5 kV
10) +/- 5.0 kV

Every CUT is only stressed with impulses of a single polarity. Necessarily, at least two CUT samples have to be tested to cover the whole voltage range from -5.0 kV to +5.0 kV. However, four CUT samples per polarity, meaning eight CUTs in total were used for each test sequence. Every single stress voltage level is applied to the CUT multiple

times within the same stressing step. After that, the stressing is stopped and the CUT is taken to be measured, before the next stressing step with an increased stress voltage level is commenced. The actual number of ESD impulses applied to the CUT during a single stressing step is constant for a whole sequence. For the results presented here, either ten or five ESD impulses were applied to the CUT per stress voltage level.

IV. Derating of the Capacitors

During the measurement steps mentioned above, the impedance analyser reads the capacitance of the CUT over a frequency range. However, only the capacitance at a fixed frequency is evaluated within the subsequent analysis. This fixed frequency was chosen with 13.75 MHz for the capacitance of the CUTs investigated for this presentation. Main concern in finding this frequency was to avoid resonance frequencies of the CUTs on the one hand side, while also providing information about the derating of the RF characteristics of the CUT on the other hand side.

After an ESD and measurement sequence has finished, the capacitance values are plotted over the individual stress voltages. Every graph is then normalised with respect to the zero-voltage capacitance. This improves the readability of the graphs, since every real capacitor comes with a certain tolerance concerning its nominal capacitance value. Since the variation of the capacitance value of mass produced capacitors is not subject of this investigation, the normalisation is used to remove this offset.

Eight sequences with different CUTs are made to constitute one plot, as shown below. Precisely, four samples are stressed with positive polarity voltages, and four other samples are stressed with negative polarity. Two statistical curves are added to the resulting set of curves:

1) Median values (bold black)
2) Arithmetic mean values (thin black)

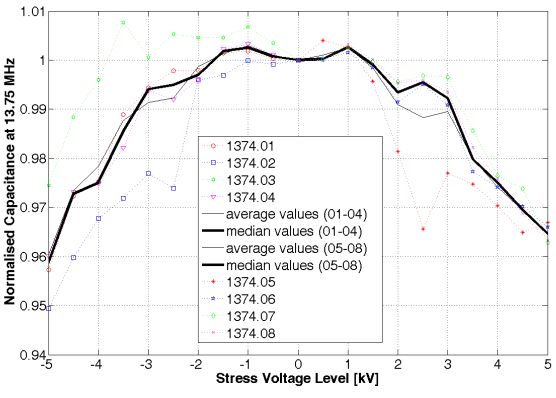

Figure 5. Normalised capacitance value at 13.75 MHz vs. stress voltage level (10 shots per level) for sample type 1374. Four samples were used for each polarity, all measurements are normalised on the respective initial zero voltage values of the sample.

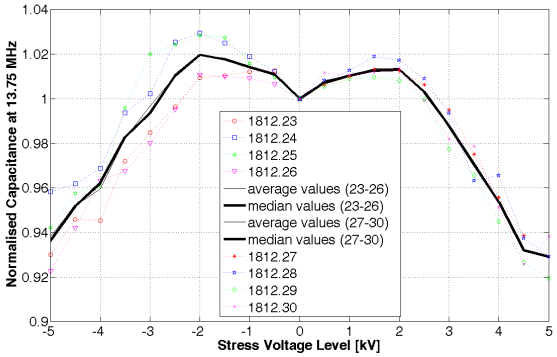

Figure 6. Normalised capacitance value at 13.75 MHz vs. stress voltage level (5 shots per level) for sample type 1812. Four samples were used for each polarity, all measurements are normalised on the respective initial zero voltage values of the sample.

Fig. 5 shows such a set of curves for sample type 1374, where the numbering of the sample types was chosen arbitrarily and does not refer to certain characteristics of the CUT. However, individual samples of the same make are numbered individually after the type number. For example, 1374.05 refers to CUT sample number five of the 1374 type.

For Fig. 5 the number of ESD impulses applied to the CUT during the stressing steps was ten. While the mean values show symmetrical characteristics over voltage magnitude, single samples provide outliers at certain voltages, 1374.05 at +2.5 kV, for example. But even in such different characteristics there can be found symmetry, as for sample 1374.02 at -2.5 kV also can be found a local minimum.

For the samples in Fig. 5 which were stressed with negative polarity the confidence interval (not indicated in Fig. 5) of the mean values is more than twice the size compared to the most points for the positive voltages, although the mean values show good symmetry for each voltage polarity. These effects may become more transparent as the number of CUTs are increased in future investigations.

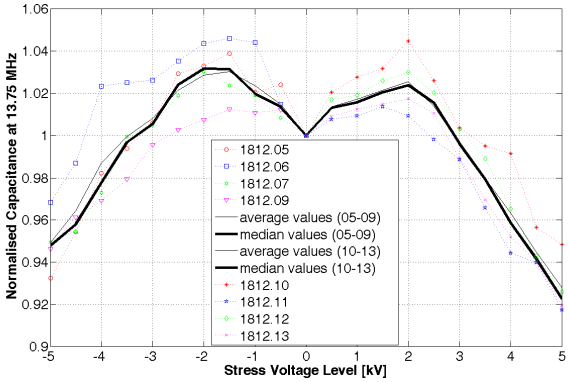

Figure 7. Normalised capacitance value at 13.75 MHz vs. stress voltage level (10 shots per level) for sample type 1812. Four samples were used for each polarity, all measurements are normalised on the respective initial zero voltage values of the sample.

A similar observation can be made for the set of curves in Fig. 6, where the negatively stressed samples' capacitance again varies more than after the positive impulses, although the number of impulses is five here for every stress voltage level of both polarities. Comparing the variation of the capacitance to Fig. 7 for which ten impulses per voltage stress level were used, yields the insight that with higher number of ESD stresses per voltage level the statistical spread of the resulting capacitance increases and the result becomes less predictable. When comparing the mean values for Fig. 6 and Fig. 7, symmetry can be stated concerning the slope of the mean curves of the two polarities, although higher capacitances are reached for the negative impulses. Higher number of impulses also raises the maximum capacitances reached around +/- 2.0 kV for the 1812 sample type.

Comparing the curves for the different sample types 1374 and 1812 shows that the 1812 type in fact has different derating behaviour in that its capacitances can be raised by an average of +3 % for stress impulses of around +/- 2.0 kV, which is not the case for the 1374 sample types where not even +1 % of increase can be found for individual samples.

In terms of minumum values the 1812 capacitor make also proves more robust towards ESD compared to the 1374 type. Whereas for the 1374 a decrease of the relative capacitance amounts to -5 %, the 1812 capacitors decrease down to -8 % from their initial value.

V. Conclusion

This paper presents the derating of ceramic capacitors after being stressed with multiple electrostatic discharges from an ISO ESD simulator gun.

As a general observation, it can be stated that the capacitance of a ceramic capacitor decreases towards higher stress voltages, since all minima are found at the maximum voltages of both polarities.

Furthermore the interval of possible capacitance values due to ESD varies between the different types of capacitors investigated. When defining a robustness towards ESD, it makes sense to say, that the smaller this interval is, the higher the robustness of a capacitor is.

In the examples provided above, the 1374 samples' capacitances spanned a derating interval of approximately 6 %, whereas single 1812 capacitors changed their characteristics over more than 10 % over the voltage interval considered.

References

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